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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,262	09/29/2003	Larry Thayer	200207036-1	1764

22879 7590 12/27/2005

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EXAMINER	
KO, DANIEL BOKMIN	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 12/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/674,262	THAYER ET AL.	
	Examiner	Art Unit	
	Daniel B. Ko	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/29/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is responsive to the application filed on 9/29/2003. Claims 1-17 have been submitted for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh (US Patent 6,202,133 B1) in view of Merkey (US Patent Application 2003/0070043 A1).

Regarding claims 1, 9, and 16, Jeddeloh teaches a memory system comprising:

a host integrated circuit (Fig. 1, First Process 22; column 3, lines 64-67; column 4, lines 1-2);

a first memory controller (Fig. 1, First Memory Controller 52) having at least one associated memory defining a first address space (column 4, lines 34-53);

a second memory controller (Fig. 1, Second Memory Controller 62) having at least one associated memory defining a second address space (column 4, lines 64-67).

Jeddeloh fails to teach parity information associated with the first and second memory controllers in an interleaved fashion.

Merkey teaches a parity memory for storing parity information associated with data stored in the memories associated with the first and second memory controllers (Fig. 2d, 226, page 3, paragraph 73); and a controller for the storing data in the parity memory, the controller configured to store parity data associated with data stored in the memory associated with the first memory controller in an interleaved fashion with data stored in the memory associated with the second memory controller (page 3, paragraph 73, paragraph 74, Merkey discloses a disk contains parity in interleaved fashion).

At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the Jeddeloh with Merkey. The motivation for doing so would have been a faster transaction processing (See Jeddeloh, column 5, lines 5-13). Jeddeloh states that the computer system can reduce read/write delay by storing data that are

mostly read in one of the system memory module while storing data that are mostly write in the other system memory module (column 5, lines 14-27).

Regarding claims 2 and 10, Merkey teaches a memory system, wherein the memory system is a RAID memory system (page 2, paragraph 69).

Regarding claim 3, Merkey teaches a memory system, wherein the memory system is a RAID 3 memory system (page 3, paragraph 73).

Regarding claims 4 and 11, Jeddeloh teaches a memory system, wherein the first and second memory controllers are capable of being configured to define the first and second address spaces to be non-overlapping (column 5, lines 28-44).

Regarding claims 5, 12, and 17, Jeddeloh teaches a memory system, wherein an address bit is appended to a plurality of address bits used to store and retrieve parity information in the parity memory, wherein the appended address bit is set to a first value when storing and retrieving parity information associated with the first memory controller (column 5, lines 55-67; column 6, lines 1-3; Jeddeloh discloses address having zero for bit if transaction is directed to the first memory module) and the appended address bit is set to a second value when storing and retrieving parity information associated with the second memory controller (column 6, lines 1-3;

Jeddeloh discloses address having one for bit if transaction is directed to the second memory module).

Regarding claims 6 and 13, Merkey teaches a memory system, wherein the memory associated with the first memory controller and the memory associated with the second memory controller are different sizes (page 9, paragraph 127).

Regarding claims 7 and 14, Merkey teaches a memory system, wherein the parity memory is at least as large as the larger of the memory associated with the first memory controller and the memory associated with the second memory controller (page 9, paragraph 128).

Regarding claims 8 and 15, Merkey teaches a memory system, wherein there are two memory busses associated with the first memory controller, two memory busses associated with the second memory controller, and two parity memory busses (Fig. 2d, page 3, paragraph 73; it is clear that two memory busses associated with the first memory controller because one is connected to host process and other is connected to party memory controller. Second memory controller is same. Also, it is clear two parity busses required because one is connected to first memory controller and other is connected to second memory controller).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel B. Ko whose telephone number is 571-272-8194.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manorama Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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